

Commissioner for Patents
Reply to Office Action of July 7, 2005
Page 3

Serial No.: 10/730,002

AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. Canceled.
2. (Currently Amended) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:
a first dynamic logic stage having an evaluate clock logic circuit comprising at least first and second ~~The domino logic circuit as claimed in claim 1 wherein the~~ transistors comprise n-mosfet transistors respectively driven by separate phases of the multi-phase clock.
3. (Currently amended) The domino logic circuit as claimed in claim 1-2 wherein the first and second transistors are connected to perform any one of:
a logical OR-function of a current clock phase and a next clock phase;
a logical AND-function of ~~a~~ the current clock phase and a previous clock phase.
4. (Currently amended) The domino logic circuit as claimed in claim 1-2, wherein the dynamic logic stage further comprises a precharge clock logic circuit ~~having comprising~~ comprising at least first and second ~~p-mosfet~~ p-mosfet transistors respectively driven by ~~respective-separate~~ phases of the multi-phase clock ~~signals~~.
5. (Currently amended) The domino logic circuit as claimed in claim 1-2, wherein the first dynamic logic ~~gate stage~~ stage comprises any one of:
an input complemented logic gate;
a non-monotonic logic gate; and
a standard dynamic logic gate.
6. (Currently amended) The domino logic circuit as claimed in claim 5, further comprising a plurality of logic phases connected in series, each logic phase comprising a respective first logic ~~gate~~ stage.

BEST AVAILABLE COPY

Commissioner for Patents
Reply to Office Action of July 7, 2005
Page 4

Serial No.: 10/730,002

7. (Currently amended) The domino logic circuit as claimed in claim 6, wherein at least one logic phase further comprises a second logic gate connected in series with the respective first dynamic logic gatestage.
8. (Previously Presented) The domino circuit as claimed in claim 7, wherein the second logic gate comprises either one of:
 - a static logic gate; and
 - a standard dynamic logic gate.
9. (Currently amended) A single-rail domino circuit driven in accordance with a multi-phase clock, comprising:
 - a plurality of logic phases connected in series, each logic phase being respectively associated with a ~~respective~~ current clock phase and comprising at least one dynamic logic gate;
 - a respective evaluate clock logic circuit connected to control an evaluate cycle of each ~~dynamic logic gate~~ logic phase, the evaluate clock logic circuit comprising respective first and second n-mosfet transistors respectively connected to receive ~~the respective one of~~ a current clock phase and an adjacent clock phase, such that overlap between a precharge cycle of a first logic phase and an evaluation cycle of an adjacent logic phase is prevented.
10. (Previously Presented) A single-rail domino circuit as claimed in claim 9, wherein a first dynamic logic gate lies on a boundary between its respective logic phase and a previous logic phase, and comprises any one of:
 - an input complemented logic gate;
 - a non-monotonic logic gate; and
 - a standard dynamic logic gate.
11. (Previously Presented) A single-rail domino circuit as claimed in claim 10, wherein the first dynamic logic gate is connected in series with a second logic gate within the same logic phase, the second logic gate comprising either one of:
 - a static logic gate; and
 - a standard dynamic logic gate.

BEST AVAILABLE COPY

Commissioner for Patents
Reply to Office Action of July 7, 2005
Page 5

Serial No.: 10/730,002

12. (Currently Amended) A single-rail domino circuit as claimed in claim 9, wherein the first and second n-mosfet transistors are connected to perform any one of:
- a logical OR-function of the respective current clock phase and a next clock phase;
 - a logical AND-function of the respective current clock phase and a previous clock phase.
13. (New) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:
- a first dynamic logic stage comprising a precharge clock logic circuit comprising at least one p-mosfet transistor respectively driven by a separate phase of the multi-phase clock; and
 - a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock.
14. (New) The domino logic circuit as claimed in claim 13 wherein the first dynamic logic stage comprises two p-mosfet transistors driven by separate phases of the multi-phase clock.
15. (New) The domino logic circuit as claimed in claim 13 wherein the second dynamic logic stage comprises two n-mosfet transistors driven by separate phases of the multi-phase clock.
16. (New) The domino logic circuit as claimed in claim 13 wherein:
- the first dynamic logic stage performs any one of:
 - an OR-precharge function;
 - a domino-precharge function; and
 - the second dynamic logic stage performs any one of:
 - an AND-evaluate function;
 - an OR-evaluate function; and
 - a domino-evaluate function.

BEST AVAILABLE COPY

Commissioner for Patents
Reply to Office Action of July 7, 2005
Page 6

Serial No.: 10/730,002

17. (New) The domino logic circuit as claimed in claim 14 comprising dynamic gates directly coupled back-to-back at cell boundaries without an intervening static gate and the domino logic circuit performs a dynamic cascaded OR-precharge/domino-evaluate function.
18. (New) The domino logic circuit as claimed in claim 14 comprising dynamic gates directly coupled back-to-back at cell boundaries without an intervening static gate and the domino logic circuit performs a dynamic cascaded domino-precharge/AND-evaluate function.
19. (New) The domino logic circuit as claimed in claim 13 further comprising a secondary precharge network, comprising:
at least one p-mosfet transistor respectively driven by the separate phase of the multi-phase clock.
20. (New) The domino logic circuit as claimed in claim 14 further comprising a secondary precharge network, comprising:
two p-mosfet transistors respectively driven by the separate phases of the multi-phase clock.

BEST AVAILABLE COPY